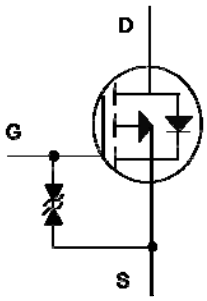
杰力科技股份有限公司
Excelliance MOS Corporation

EMZB08P03H

P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DSON\ (MAX.)}$	8.5mΩ
I_D	-70A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ESD Protection

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	-70	A
	T_C = 100 °C		-50	
Pulsed Drain Current[1]		I_{DM}	-150	
Avalanche Current		I_{AS}	-50	
Avalanche Energy	L = 0.1mH, I_D=-50A, R_G=25Ω	E_{AS}	125	mJ
Power Dissipation	T_C = 25 °C	P_D	50	W
	T_C = 100 °C		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=-15V, L=0.1mH, V_G=-10V, I_L=-40A, Rated V_{DS}=-30V P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.5	-3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-70			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -15A		7	8.5	mΩ
		V_{GS} = -4.5V, I_D = -12A		12	15	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -15A		26		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		3091		pF
Output Capacitance	C_{oss}			476		
Reverse Transfer Capacitance	C_{rss}			404		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		3.5		Ω
Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	V_{DS} = -15V, V_{GS} = -10V, I_D = -15A		54		nC
	Q_g(V_{GS}=4.5V)			32		
Gate-Source Charge[1,2]	Q_{gs}			7.3		
Gate-Drain Charge[1,2]	Q_{gd}			13		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -15V, I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7Ω		24		nS
Rise Time[1,2]	t_r			20		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			70		
Fall Time[1,2]	t_f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-70	A
Pulsed Current[3]	I_{SM}				-150	
Forward Voltage[1]	V_{SD}	I_F = -15A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS		52		nS
Reverse Recovery Charge	Q_{rr}			60		nC

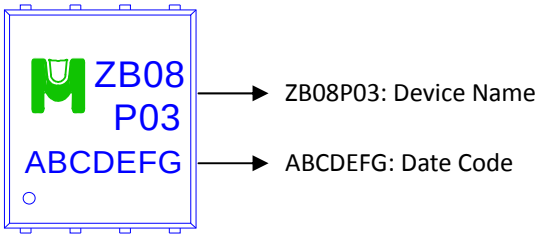
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

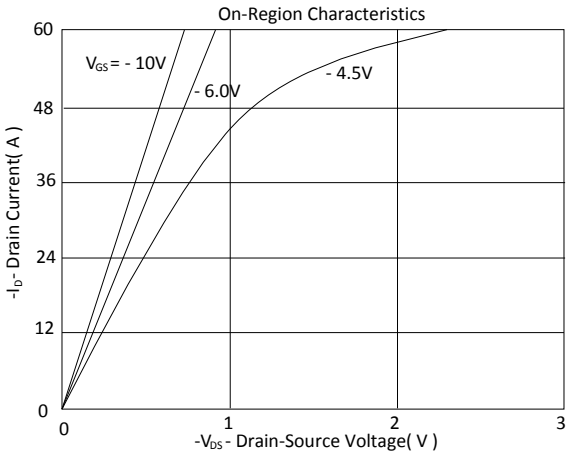
[2]Independent of operating temperature.

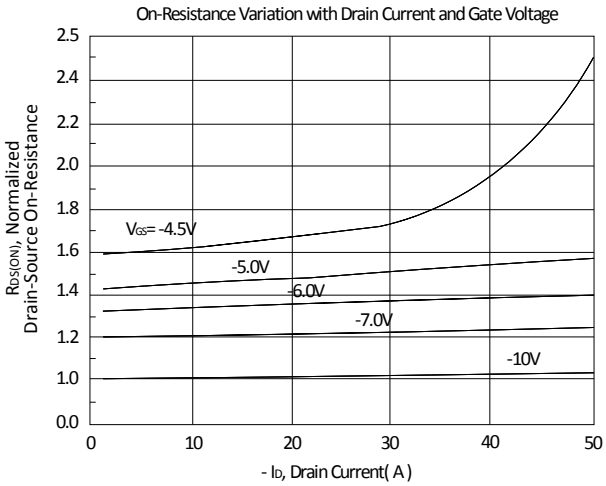
[3]Pulse width limited by maximum junction temperature.

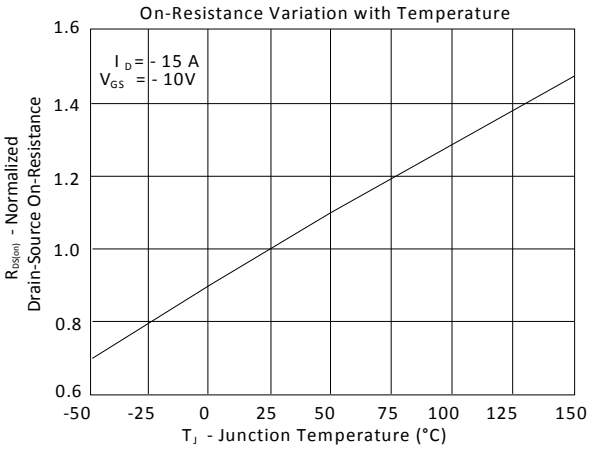
Ordering & Marking Information:

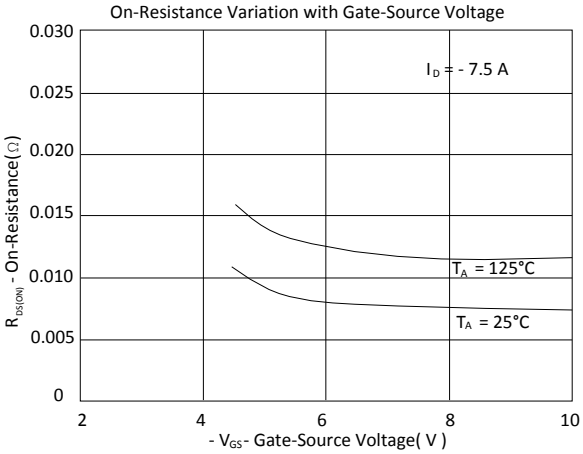
Device Name: EMZB08P03H for EDFN 5 x 6

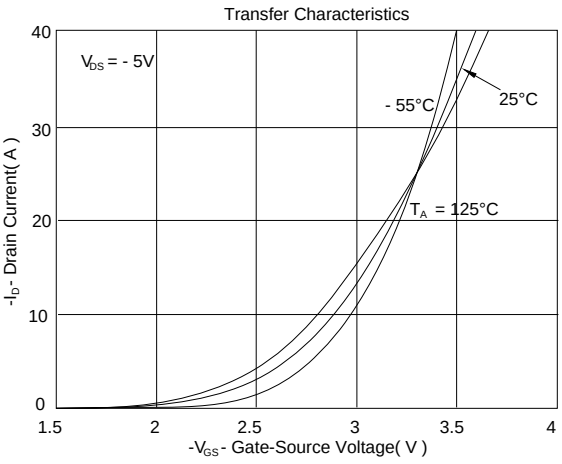


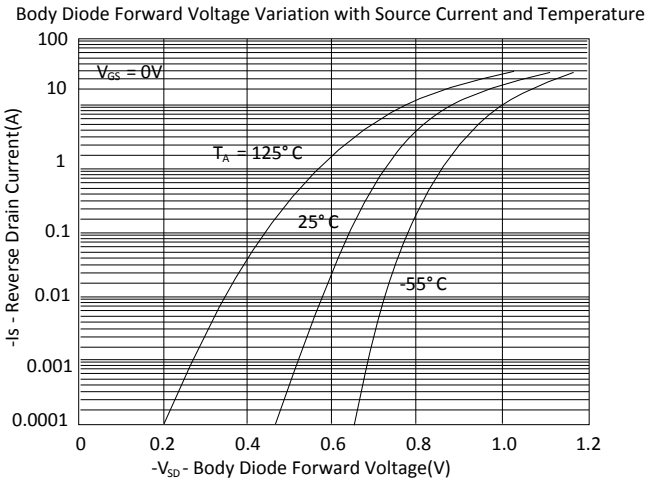

On-Region Characteristics
V_{GS} = - 10V
- 6.0V
- 4.5V
-I_D- Drain Current(A)
-V_{DS}- Drain-Source Voltage(V)

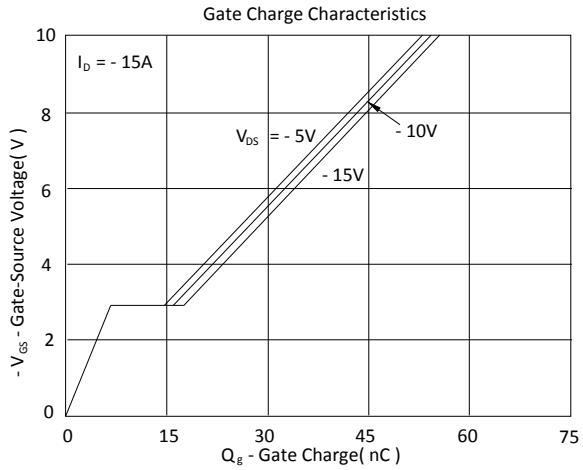

On-Resistance Variation with Drain Current and Gate Voltage
$R_{DS(ON)}$, Normalized
Drain-Source On-Resistance
V_{GS}= -4.5V
-5.0V
-6.0V
-7.0V
-10V
- I_D, Drain Current(A)

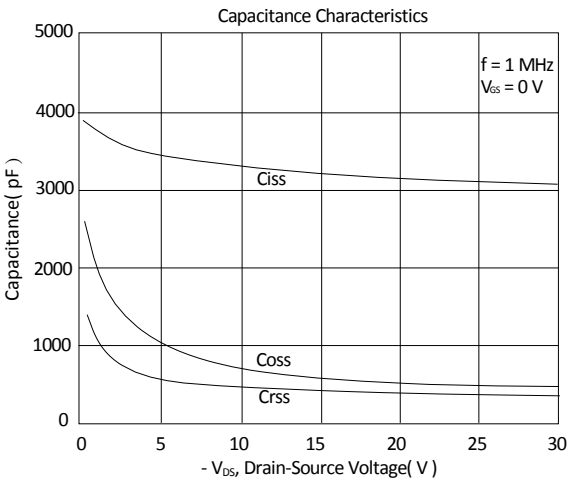

On-Resistance Variation with Temperature
I_D = - 15 A
V_{GS} = - 10V
$R_{DS(on)}$ - Normalized
Drain-Source On-Resistance
T_J - Junction Temperature (°C)

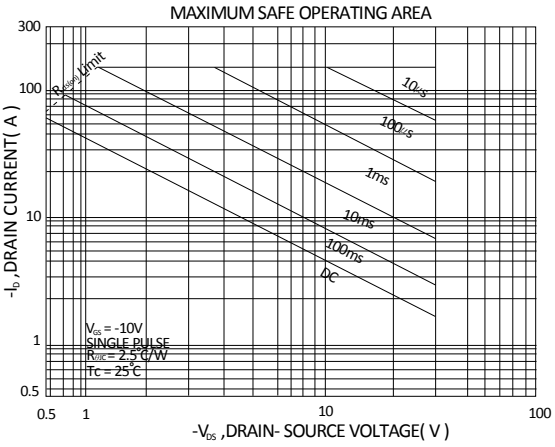

On-Resistance Variation with Gate-Source Voltage
I_D = - 7.5 A
T_A = 125°C
T_A = 25°C
$R_{DS(ON)}$ - On-Resistance(Ω)
- V_{GS}- Gate-Source Voltage(V)

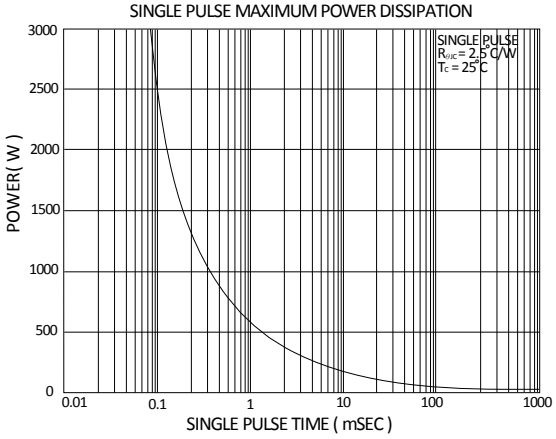

Transfer Characteristics
V_{DS} = - 5V
- 55°C
25°C
T_A = 125°C
-I_D- Drain Current(A)
-V_{GS}- Gate-Source Voltage(V)

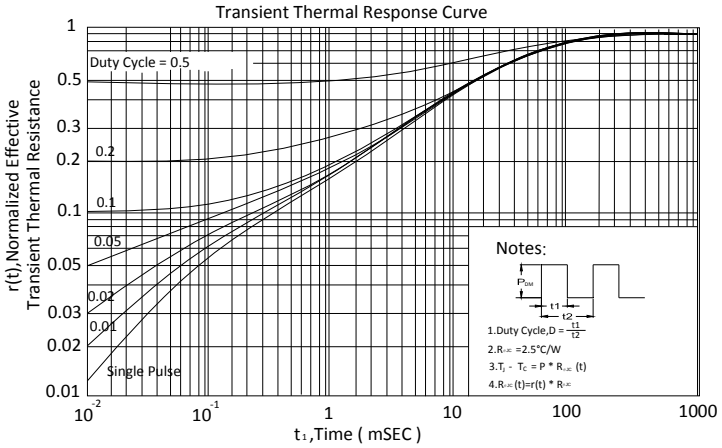

Body Diode Forward Voltage Variation with Source Current and Temperature
V_{GS} = 0V
T_A = 125° C
25° C
-55° C
-Is - Reverse Drain Current(A)
-V_{SD} - Body Diode Forward Voltage(V)


Gate Charge Characteristics
I_D = - 15A
V_{DS} = - 5V
- 10V
- 15V
- V_{GS} - Gate-Source Voltage(V)
Q_g - Gate Charge(nC)

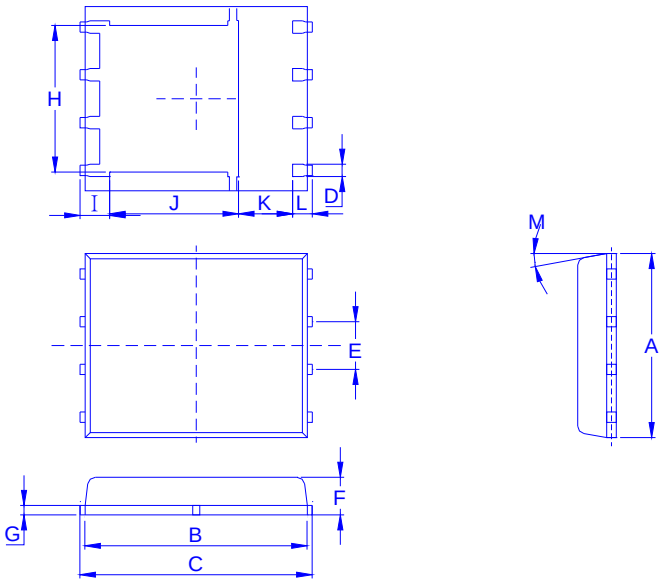

Capacitance Characteristics
f = 1 MHz
V_{GS} = 0 V
Ciss
Coss
Crss
Capacitance(pF)
- V_{DS}, Drain-Source Voltage(V)


MAXIMUM SAFE OPERATING AREA
$R_{DS(on)}$ Limit
10μs
100μs
1ms
10ms
100ms
DC
V_{GS} = -10V
SINGLE PULSE
$R_{\theta JC}$ = 2.5°C/W
Tc = 25°C
-I_D ,DRAIN CURRENT(A)
-V_{DS} ,DRAIN- SOURCE VOLTAGE(V)


SINGLE PULSE MAXIMUM POWER DISSIPATION
SINGLE PULSE
$R_{\theta JC}$ = 2.5°C/W
T_C = 25°C
POWER(W)
SINGLE PULSE TIME (mSEC)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D = t1/t2
2.$R_{\theta JC}$ =2.5°C/W
3.T_J - T_C = P * $R_{\theta JC}$ (t)
4.$R_{\theta JC}$ (t)=r(t) * $R_{\theta JC}$
r(t),Normalized Effective Transient Thermal Resistance
t_1 ,Time (mSEC)

Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads