Dual Synchronous, Step-Down Controller with 5-V and 3.3-V LDOs

Check for Samples: TPS51225, TPS51225B, TPS51225C

FEATURES

- **Input Voltage Range: 5.5 V to 24 V**
- **Output Voltages: 5 V and 3.3 V (Adjustable Range ±10%)**
- **Built-in, 100-mA, 5-V and 3.3-V LDOs**
- **Clock Output for Charge-Pump**
- **±1% Reference Accuracy**
- **Adaptive On-time D-CAP™ Mode Control Architecture with 300kHz/355kHz Frequency Setting**
- **Auto-skip Light Load Operation (TPS51225/C)**
- **OOA Light Load Operation (TPS51225B)**
- **Internal 0.8-ms Voltage Servo Soft-Start**
- **Low-Side $R_{DS(on)}$ Current Sensing Scheme with 4500 ppm/°C Temperature Coefficient**
- **Built-in Output Discharge Function**
- **Separate Enable Input for Switchers (TPS51225/B/C)**
- **Dedicated OC Setting Terminals**
- **Power Good Indicator**
- **OVP/UVP/OCP Protection**
- **Non-latch UVLO/OTP Protection**
- **20-Pin, 3 mm × 3 mm, QFN (RUK)**

APPLICATIONS

- **Notebook Computers**
- **Netbook, Tablet Computers**

DESCRIPTION

The TPS51225/B/C is a cost-effective, dual-synchronous buck controller targeted for notebook system-power supply solutions. It provides 5-V and 3.3-V LDOs and requires few external components. The 260-kHz VCLK output can be used to drive an external charge pump, generating gate drive voltage for the load switches without reducing the main converter efficiency. The TPS51225/B/C supports high efficiency, fast transient response and provides a combined power-good signal. Adaptive on-time, D-CAP™ control provides convenient and efficient operation. The device operates with supply input voltage ranging from 5.5 V to 24 V and supports output voltages of 5.0 V and 3.3 V. The TPS51225/B/C is available in a 20-pin, 3 mm × 3 mm, QFN package and is specified from –40°C to 85°C.

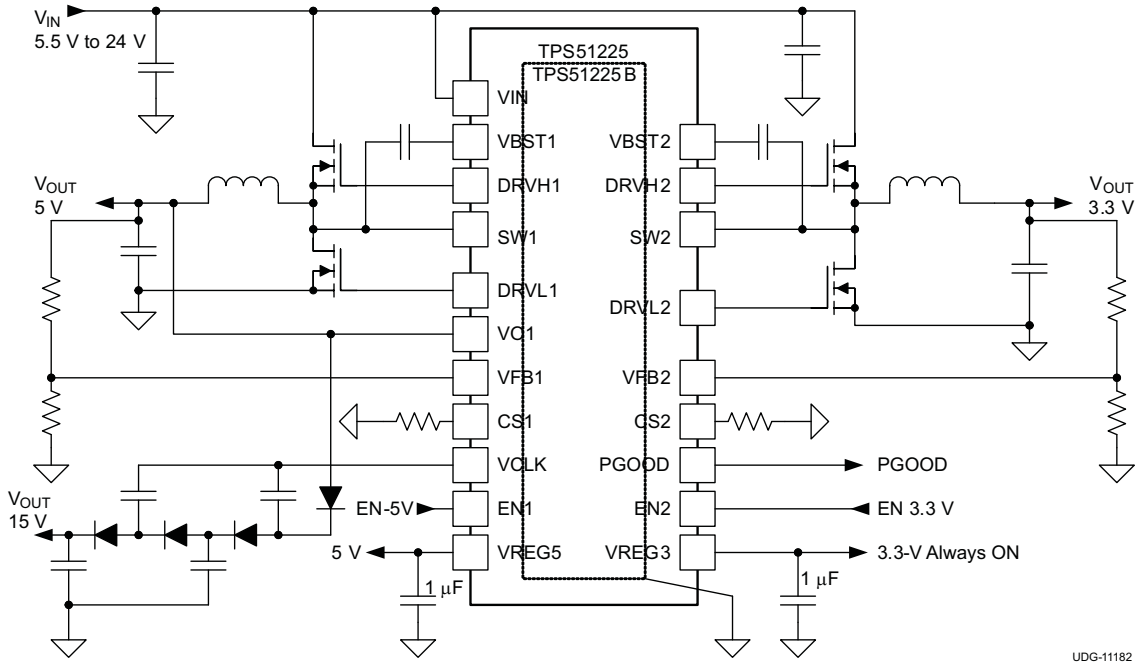
ORDERING INFORMATION(1)

ORDERABLE DEVICE NUMBER	ENABLE FUNCTION	SKIP MODE	ALWAYS ON-LDO	PACKAGE	OUTPUT SUPPLY	QUANTITY
TPS51225RUKR	EN1/ EN2	Auto-skip	VREG3	PLASTIC Quad Flat Pack (20 pin QFN)	Tape and Reel	3000
TPS51225RUKT					Mini reel	250
TPS51225BRUKR	EN1/ EN2	OOA	VREG3		Tape and Reel	3000
TPS51225BRUKT					Mini reel	250
TPS51225CRUKR	EN1/ EN2	Auto-skip	VREG3 & VREG5		Tape and Reel	3000
TPS51225CRUKT					Mini reel	250

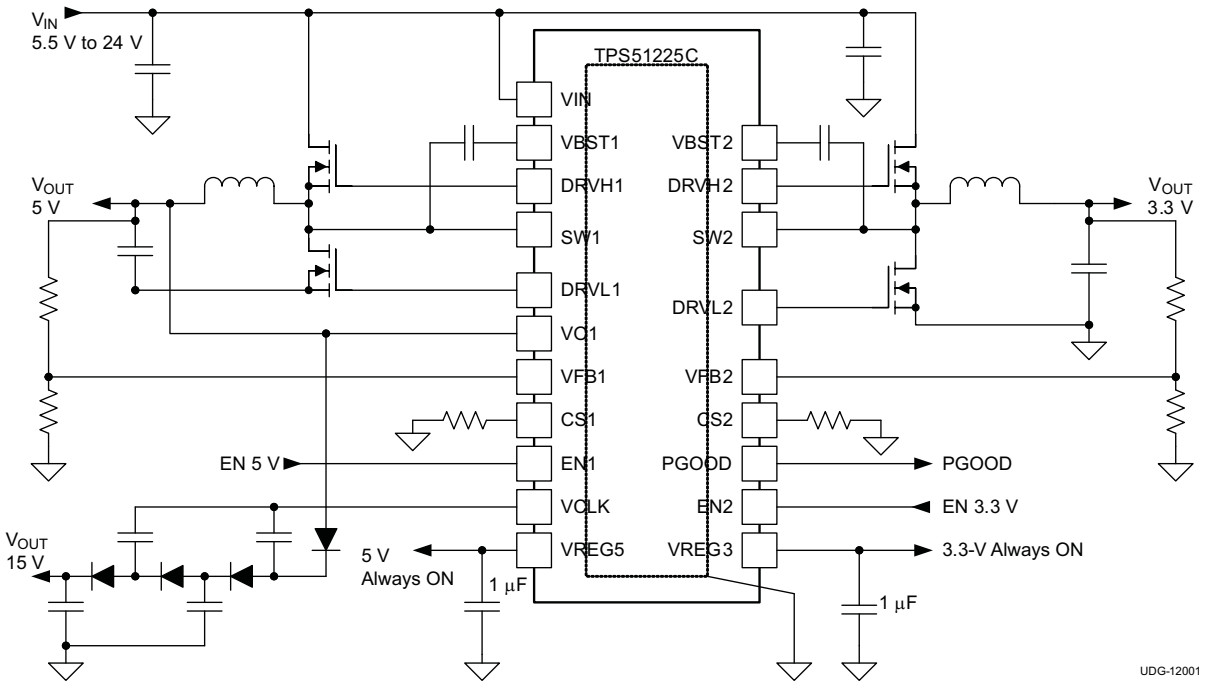
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION DIAGRAM (TPS51225/TPS51225B)



TYPICAL APPLICATION DIAGRAM (TPS51225C)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage(2)	VBST1, VBST2	–0.3	32	V
	VBST1, VBST2(3)	–0.3	6	
	SW1, SW2	–6.0	26	
	VIN	–0.3	26	
	EN1, EN2	–0.3	6	
	VFB1, VFB2	–0.3	3.6	
	VO1	–0.3	6	
Output voltage(2)	DRVH1, DRVH2	–6.0	32	V
	DRVH1, DRVH2(3)	–0.3	6	
	DRVH1, DRVH2(3) (pulse width < 20 ns)	–2.5	6	
	DRVL1, DRVL2	–0.3	6	
	DRVL1, DRVL2 (pulse width < 20 ns)	–2.5	6	
	PGOOD, VCLK, VREG5	–0.3	6	
	VREG3, CS1, CS2	–0.3	3.6	
Electrostatic discharge	HBM QSS 009-105 (JESD22-A114A)		2	kV
	CDM QSS 009-147 (JESD22-C101B.01)		1	
Junction temperature, T_J		150		°C
Storage temperature, T_{ST}		–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted
(3) Voltage values are with respect to SW terminals.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51225 TPS51225B TPS51225C	UNITS
		20-PIN RUK	
θ_{JA}	Junction-to-ambient thermal resistance	94.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	58.1	
θ_{JB}	Junction-to-board thermal resistance	64.3	
ψ_{JT}	Junction-to-top characterization parameter	31.8	
ψ_{JB}	Junction-to-board characterization parameter	58.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	VIN	5.5		24	V
Input voltage(1)	VBST1, VBST2	–0.1		30	V
	VBST1, VBST2(2)	–0.1		5.5	V
	SW1, SW2	–5.5		24	V
	EN1, EN2	–0.1		5.5	V
	VFB1, VFB2	–0.1		3.5	V
	VO1	–0.1		5.5	V
Output voltage(1)	DRVH1, DRVH2	–5.5		30	V
	DRVH1, DRVH2(2)	–0.1		5.5	V
	DRVL1, DRVL2	–0.1		5.5	V
	PGOOD, VCLK, VREG5	–0.1		5.5	V
	VREG3, CS1, CS2	–0.1		3.5	V
Operating free-air temperature, T_A		–40		85	°C

(1) All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) Voltage values are with respect to the SW terminal.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{VIN}= 12 V, V_{VO1}= 5 V, V_{VFB1}= V_{VFB2}= 2 V, V_{EN1}= V_{EN2}= 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{VIN1}	VIN supply current-1	T_A = 25°C, No load, V_{VO1}=0 V			860		µA
I_{VIN2}	VIN supply current-2	T_A = 25°C, No load			30		µA
I_{VO1}	VO1 supply current	T_A = 25°C, No load, V_{VFB1}= V_{VFB2}=2.05 V			900		µA
$I_{VIN(STBY)}$	VIN stand-by current	T_A = 25°C, No load, V_{VO1}= 0 V, V_{EN1}= V_{EN2}= 0 V	TPS51225 TPS51225B		95		µA
$I_{VIN(STBY)}$	VIN stand-by current	T_A = 25°C, No load, V_{VO1}=0 V, V_{EN1}=V_{EN2}=0V (TPS51225C)			180		µA
INTERNAL REFERENCE							
V_{FBx}	VFB regulation voltage	T_A = 25°C		1.99	2.00	2.01	V
				1.98	2.00	2.02	V
VREG5 OUTPUT							
V_{VREG5}	VREG5 output voltage	No load, V_{VO1}= 0 V, T_A = 25°C		4.9	5.0	5.1	V
		V_{VIN}> 7 V , V_{VO1}= 0 V, I_{VREG5}< 100 mA		4.85	5.00	5.10	
		V_{VIN} > 5.5 V , V_{VO1}= 0 V, I_{VREG5}< 35 mA		4.85	5.00	5.10	
I_{VREG5}	VREG5 current limit	V_{VIN}= 7 V, V_{VO1}= 0 V, V_{VREG5}= 4.5 V		100	150		mA
R_{V5SW}	5-V switch resistance	V_{VO1}= 5 V, I_{VREG5}= 50 mA, T_A = 25°C			1.8		Ω
VREG3 OUTPUT							
V_{VREG3}	VREG3 output voltage	No load, V_{VO1}= 0 V, T_A = 25°C		3.267	3.300	3.333	V
		V_{VIN} > 7 V , V_{VO1}= 0 V, I_{VREG3}< 100 mA		3.217	3.300	3.383	
		5.5 V < V_{VIN} , V_{VO1}= 0 V, I_{VREG3}< 35 mA		3.234	3.300	3.366	
		V_{VIN} > 5.5 V, V_{VO1} = 0 V, I_{VREG3}< 35 mA, 0°C ≤ T_A ≤ 85°C		3.267	3.300	3.333	
		V_{VIN} > 5.5 V, V_{VO1} = 5 V, I_{VREG3}< 35 mA, 0°C ≤ T_A ≤ 85°C		3.267	3.300	3.333	
I_{VREG3}	VREG3 current limit	V_{VO1}= 0 V, V_{VREG3}= 3.0 V, V_{VIN}= 7 V		100	150		mA
DUTY CYCLE and FREQUENCY CONTROL							
f_{SW1}	CH1 frequency(1)	T_A = 25°C, V_{VIN}= 20 V		240	300	360	kHz
f_{SW2}	CH2 frequency(1)	T_A = 25°C, V_{VIN}= 20 V		280	355	430	kHz
$t_{OFF(MIN)}$	Minimum off-time	T_A = 25°C		200	300	500	ns
MOSFET DRIVERS							
R_{DRVH}	DRVH resistance	Source, (V_{VBST} – V_{DRVH}) = 0.25 V, (V_{VBST} – V_{SW}) = 5 V			3.0		Ω
		Sink, (V_{DRVH} – V_{SW}) = 0.25 V, (V_{VBST} – V_{SW}) = 5 V			1.9		
R_{DRVL}	DRVL resistance	Source, (V_{VREG5} – V_{DRVL}) = 0.25 V, V_{VREG5} = 5 V			3.0		Ω
		Sink, V_{DRVL} = 0.25 V, V_{VREG5}= 5 V			0.9		
t_D	Dead time	DRVH-off to DRVL-on			12		ns
		DRVL-off to DRVH-on			20		
INTERNAL BOOT STRAP SWITCH							
$R_{VBST\ (ON)}$	Boost switch on-resistance	T_A = 25°C, I_{VBST} = 10 mA			13		Ω
I_{VBSTLK}	VBST leakage current	T_A = 25°C				1	µA
CLOCK OUTPUT							
$R_{VCLK\ (PU)}$	VCLK on-resistance (pull-up)	T_A = 25°C			10		Ω
$R_{VCLK\ (PD)}$	VCLK on-resistance (pull-down)	T_A = 25°C			10		
f_{CLK}	Clock frequency	T_A = 25°C			260		kHz

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

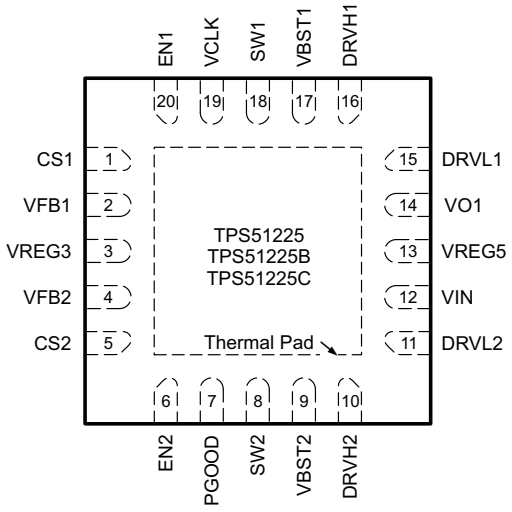
over operating free-air temperature range, V_{VIN}= 12 V, V_{VO1}= 5 V, V_{VFB1}= V_{VFB2}= 2 V, V_{EN1}= V_{EN2}= 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OUTPUT DISCHARGE						
R_{DIS1}	CH1 discharge resistance	T_A = 25°C, V_{VO1} = 0.5 V V_{EN1} = V_{EN2} = 0 V		35		Ω
R_{DIS2}	CH2 discharge resistance	T_A = 25°C, V_{SW2} = 0.5 V V_{EN1} = V_{EN2} = 0 V		75		Ω
R_{DIS2}	CH2 discharge resistance	T_A = 25°C, V_{SW2} = 0.5 V, V_{EN1} = V_{EN2} = 0 V (TPS51225C)		70		Ω
SOFT START OPERATION						
t_{SS}	Soft-start time	From ENx="Hi" and V_{VREG5} > V_{UVLO5} to V_{OUT} = 95%		0.91		ms
t_{SSRAMP}	Soft-start time (ramp-up)	V_{OUT}= 0% to V_{OUT} = 95%, V_{VREG5} = 5 V		0.78		ms
POWER GOOD						
V_{PGTH}	PG threshold	Lower (rising edge of PG-in)	92.5%	95.0%	97.5%	
		Hysteresis		5%		
		Upper (rising edge of PG-out)	107.5%	110.0%	112.5%	
		Hysteresis		5%		
I_{PGMAX}	PG sink current	V_{PGOOD} = 0.5 V		6.5		mA
I_{PGLK}	PG leak current	V_{PGOOD} = 5.5 V			1	µA
t_{PGDEL}	PG delay	From PG lower threshold (95%=typ) to PG flag high		0.7		ms
CURRENT SENSING						
I_{CS}	CS source current	T_A = 25°C, V_{CS}= 0.4 V	9	10	11	µA
TC_{CS}	CS current temperature coefficient(1)	On the basis of 25°C		4500		ppm/°C
V_{CS}	CS Current limit setting range		0.2		2	V
V_{ZC}	Zero cross detection offset	T_A = 25°C	–1	1	3	mV
LOGIC THRESHOLD						
$V_{ENX(ON)}$	EN threshold high-level	SMPS on level			1.6	V
$V_{ENX(OFF)}$	EN threshold low-level	SMPS off level	0.3			V
I_{EN}	EN input current	V_{ENx}= 3.3 V	–1		1	µA
OUTPUT OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold		112.5%	115.0%	117.5%	
t_{OVPDLY}	OVP propagation delay	T_A = 25°C		0.5		µs
OUTPUT UNDERVOLTAGE PROTECTION						
V_{UVP}	UVP trip Threshold		55%	60%	65%	
t_{UVPDLY}	UVP prop delay			250		µs
$t_{UVPENDLY}$	UVP enable delay	From ENx ="Hi", V_{VREG5} = 5 V		1.35		ms
UVLO						
$V_{UVL0VIN}$	VIN UVLO Threshold	Wake up		4.58		V
		Hysteresis		0.5		V
V_{UVLO5}	VREG5 UVLO Threshold	Wake up		4.38		V
		Hysteresis		0.4		V
V_{UVLO3}	VREG3 UVLO Threshold	Wake up		3.15		V
		Hysteresis		0.15		V
OVER TEMPERATURE PROTECTION						
T_{OTP}	OTP threshold(1)	Shutdown temperature		155		°C
		Hysteresis		10		

(1) Ensured by design. Not production tested.

DEVICE INFORMATION

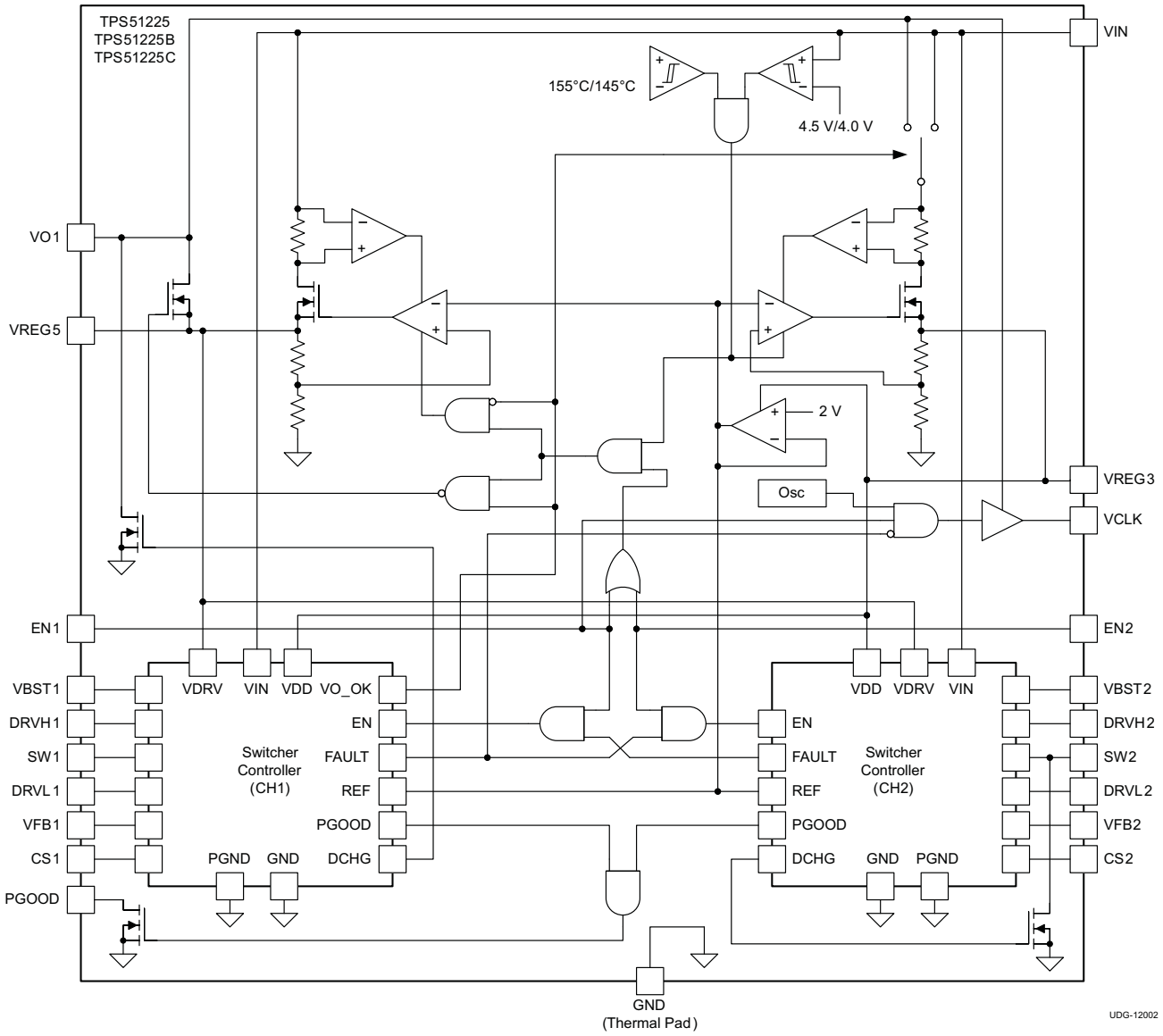
RUK PACKAGE
20 PINS
(TOP VIEW)



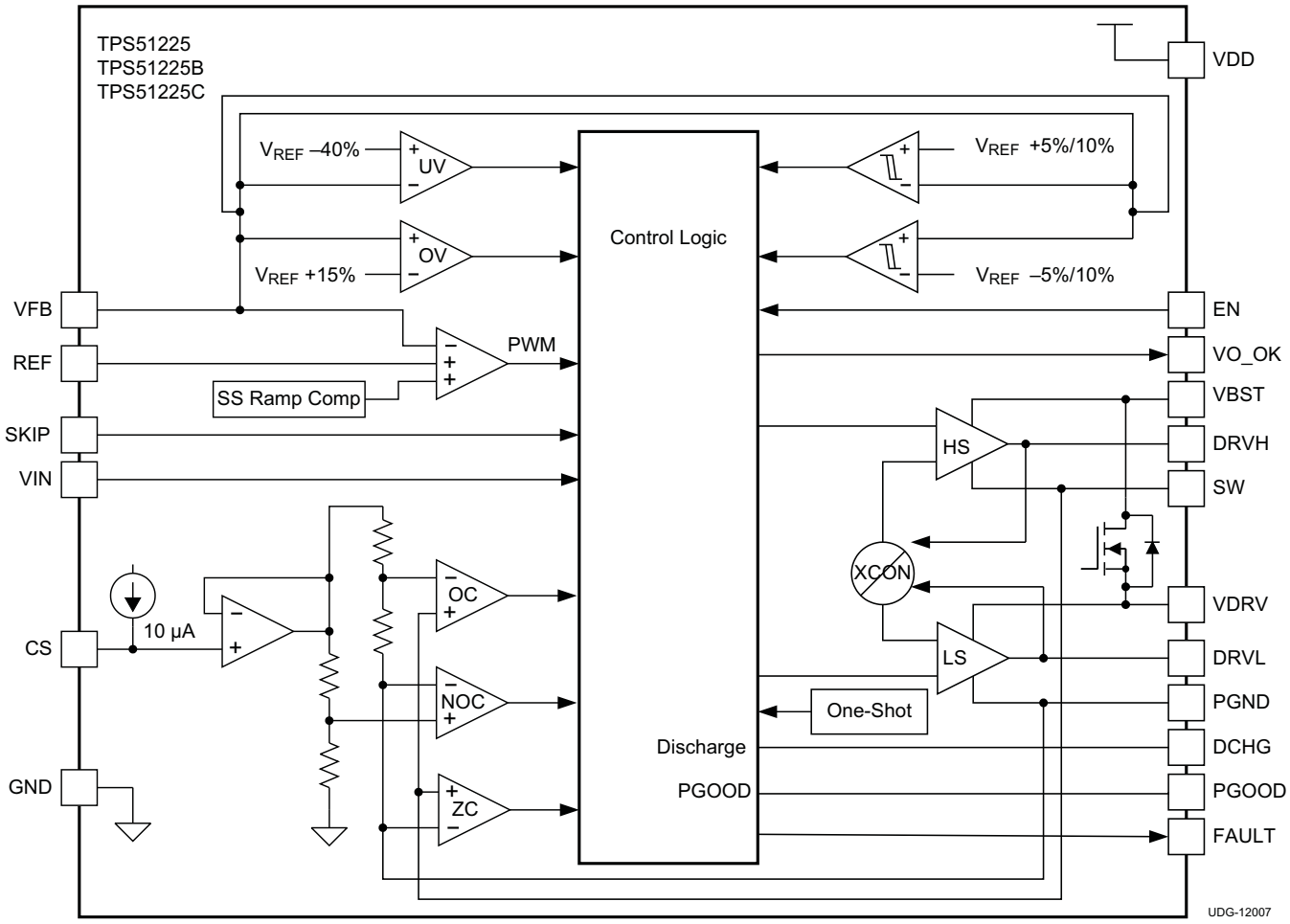
PIN FUNCTIONS

NAME	PIN NO. TPS51225 TPS51225B TPS51225C	I/O	DESCRIPTION
CS1	1	O	Sets the channel 1 OCL trip level.
CS2	5	O	Sets the channel 2OCL trip level.
DRVH1	16	O	High-side driver output
DRVH2	10	O	High-side driver output
DRVL1	15	O	Low-side driver output
DRVL2	11	O	Low-side driver output
EN1	20	I	Channel 1 enable.
EN2	6	I	Channel 2 enable.
PGOOD	7	O	Power good output flag. Open drain output. Pull up to external rail via a resistor
SW1	18	O	Switch-node connection.
SW2	8	O	Switch-node connection.
VBST1	17	I	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal.
VBST2	9	I	
VCLK	19	O	Clock output for charge pump.
VFB1	2	I	Voltage feedback Input
VFB2	4	I	
VIN	12	I	Power conversion voltage input. Apply the same voltage as drain voltage of high-side MOSFETs of channel 1 and channel 2.
VO1	14	I	Output voltage input, 5-V input for switch-over.
VREG3	3	O	3.3-V LDO output.
VREG5	13	O	5-V LDO output.
Thermal pad	—	—	GND terminal, solder to the ground plane

FUNCTIONAL BLOCK DIAGRAM (TPS51225/B/C)



SWITCHER CONTROLLER BLOCK DIAGRAM



DETAILED DESCRIPTION

PWM Operations

The main control loop of the switch mode power supply (SMPS) is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports a proprietary D-CAP™ mode. D-CAP™ mode does not require external conpensation circuit and is suitable for low external component count configuration when used with appropriate amount of ESR at the output capacitor(s).

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or enters the ON state. This MOSFET is turned off, or enters the 'OFF state, after the internal, one-shot timer expires. The MOSFET is turned on again when the feedback point voltage, V_{VFB}, decreased to match the internal 2-V reference. The inductor current information is also monitored and should be below the overcurrent threshold to initiate this new cycle. By repeating the operation in this manner, the controller regulates the output voltage. The synchronous low-side (rectifying) MOSFET is turned on at the beginning of each OFF state to maintain a minimum of conduction loss. The low-side MOSFET is turned off before the high-side MOSFET turns on at next switching cycle or when inductor current information detects zero level. This enables seamless transition to the reduced frequency operation during light-load conditions so that high efficiency is maintained over a broad range of load current.

Adaptive On-Time/ PWM Frequency Control

Bacause the TPS51225/B/C does not have a dedicated oscillator for control loop on board, switching cycle is controlled by the adaptive on-time circuit. The on-time is controlled to meet the target switching frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The target switching frequency is varied according to the input voltage to achieve higher duty operation for lower input voltage application. The switching frequency of CH1 (5-V output) is 300 kHz during continuous conduction mode (CCM) operation when V_{IN} = 20 V. The CH2 (3.3-V output) is 355 kHz during CCM when V_{IN} = 20 V.

Light Load Condition in Auto-Skip Operation (TPS51225/C)

The TPS51225/C automatically reduces switching frequency during light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without an increase in output voltage ripple. A more detailed description of this operation is as follows. As the output current decreases from heavy-load condition, the inductor current is also reduced and eventually approaches valley zero current, which is the boundary between continuous conduction mode and discontinuous conduction mode. The rectifying MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs in discontinuous conduction mode and it takes longer and longer to discharge the output capacitor to the level that requires the next ON cycle. The ON time is maintained the same as that in the heavy-load condition. In reverse, when the output current increase from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches to the continuous conduction. The transition load point to the light load operation $I_{OUT(LL)}$ (i.e. the threshold between continuous and discontinuous conduction mode) can be calculated as shown in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

where

- f_{SW} is the PWM switching frequency

Switching frequency versus output current during light-load conditions is a function of inductance (L), input voltage (V_{IN}) and output voltage (V_{OUT}), but it decreases almost proportional to the output current from the $I_{OUT(LL)}$.

Light-Load Condition in Out-of-Audio™ Operation (TPS51225B)

Out-of-Audio™ (OOA) light-load mode is a unique control feature that keeps the switching frequency above acoustic audible frequencies toward a virtual no-load condition. During Out-of-Audio™ operation, the OOA control circuit monitors the states of both MOSFETs and forces them to transition into the ON state if both of MOSFETs are off for more than 40 µs. When both high-side and low-side MOSFETs are off for 40 µs during a light-load condition, the operation mode is changed to FCCM. This mode change initiates the low-side MOSFET on and pulls down the output voltage. Then, the high-side MOSFET is turned on and stops switching again.

Table 1. SKIP Mode Operation (TPS51225/B/C)

	SKIP MODE OPERATION
TPS51225	Auto-skip
TPS51225B	OOA
TPS51225C	Auto-skip

D-CAP™ Mode

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 1.

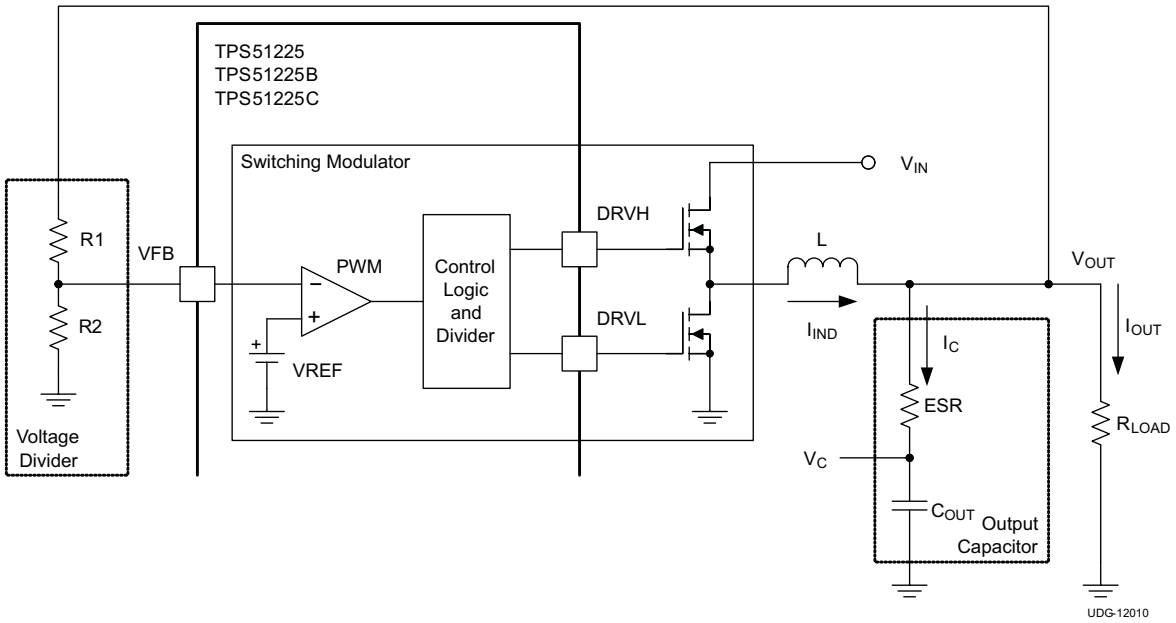


Figure 1. Simplifying the Modulator

The output voltage is compared with internal reference voltage after divider resistors, R1 and R2. The PWM comparator determines the timing to turn onthe high-side MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each ON cycle substantially constant. For the loop stability, the 0dB frequency, f_0, defined in Equation 2 must be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \le \frac{f_{SW}}{4} \quad (2)$$

As f_0 is determined solely by the output capacitor characteristics, the loop stability during D-CAP™ mode is determined by the capacitor chemistry. For example, specialty polymer capacitors have output capacitance in the order of several hundred micro-Farads and ESR in range of 10 milli-ohms. These yield an f_0 value on the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this operational mode.

Enable and Powergood

VREG3 is an always-on regulator (TPS51225/B), VREG3/VREG5 are always-on regulators (TPS51225C), when the input voltage is beyond the UVLO threshold it turns ON. VREG5 is turned ON when either EN1 or EN2 enters the ON state. The VCLK signal initiates when EN1 enters the ON state (TPS51225/B/C). Enable states are shown in Table 2 through Table 3.

Table 2. Enabling/PGOOD State (TPS51225/B)

EN1	EN2	VREG5	VREG3	CH1 (5Vout)	CH2 (3.3Vout)	VCLK	PGOOD
OFF	OFF	OFF	ON	OFF	OFF	OFF	Low
ON	OFF	ON	ON	ON	OFF	ON	Low
OFF	ON	ON	ON	OFF	ON	OFF	Low
ON	ON	ON	ON	ON	ON	ON	High

Table 3. Enabling/PGOOD State (TPS51225C)

EN1	EN2	VREG5	VREG3	CH1 (5Vout)	CH2 (3.3Vout)	VCLK	PGOOD
OFF	OFF	ON	ON	OFF	OFF	OFF	Low
ON	OFF	ON	ON	ON	OFF	ON	Low
OFF	ON	ON	ON	OFF	ON	OFF	Low
ON	ON	ON	ON	ON	ON	ON	High

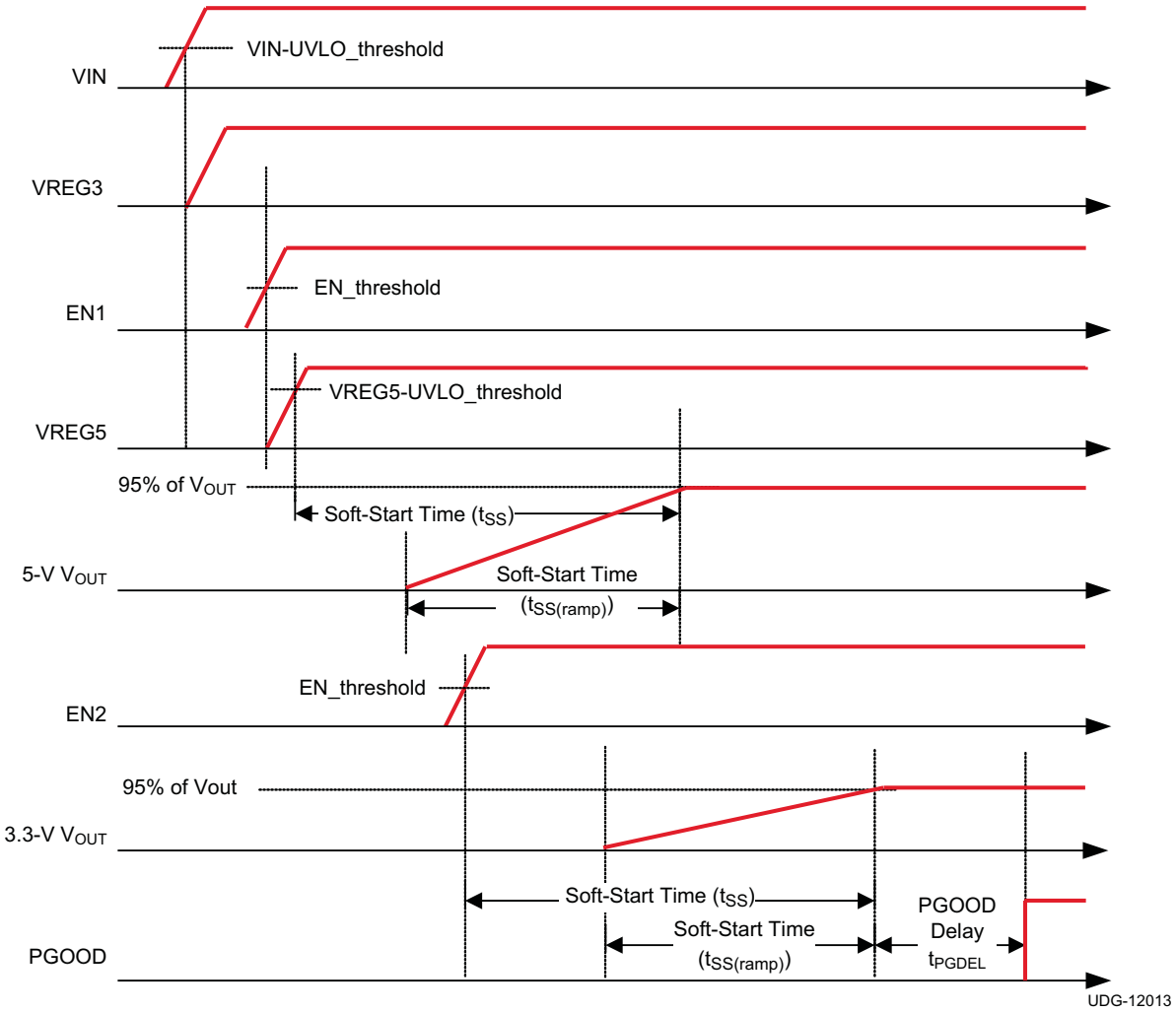


Figure 2. TPS51225 and TPS51225B Timing

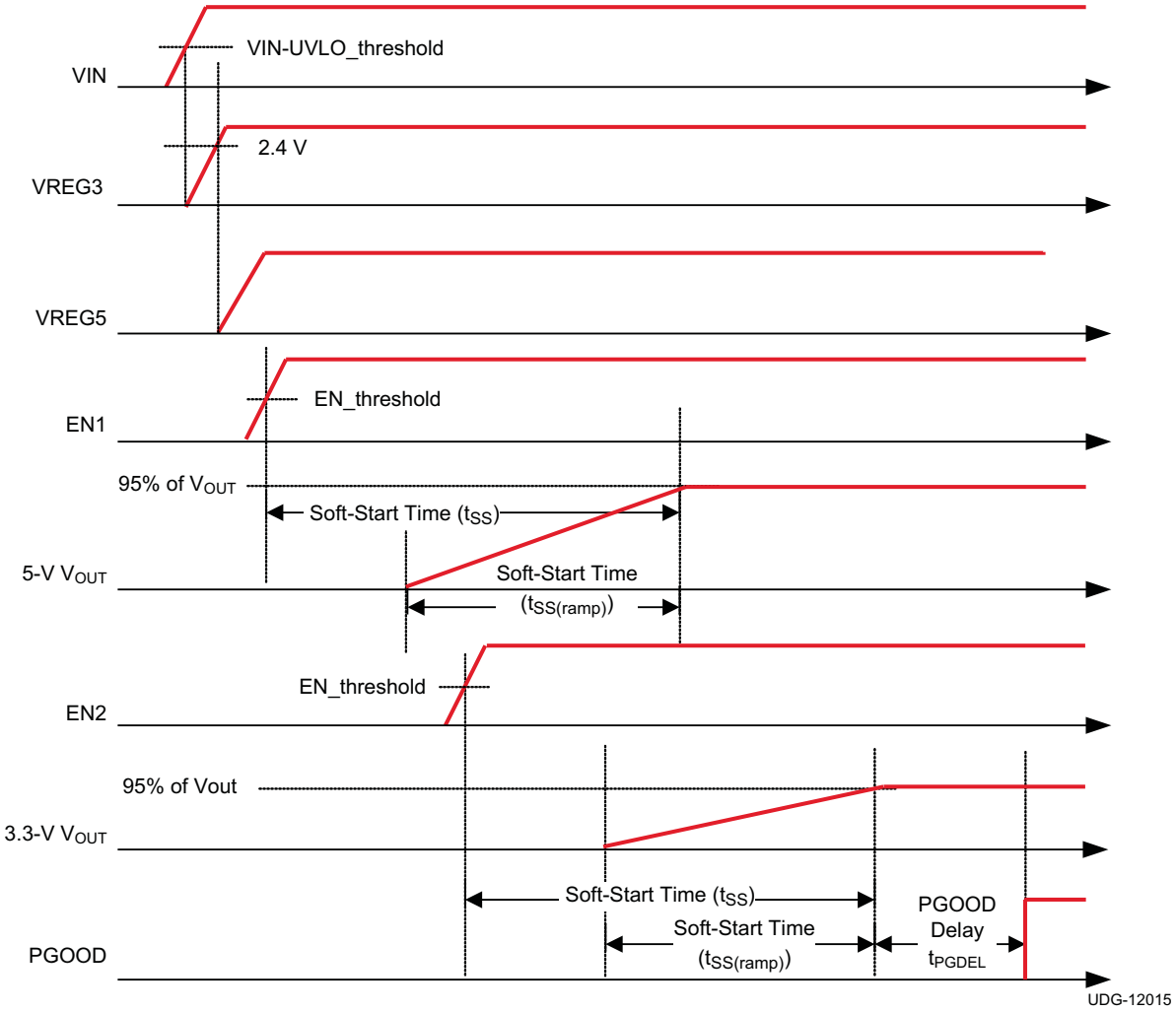


Figure 3. TPS51225C Timing

Soft-Start and Discharge

The TPS51225/B/C operates an internal, 0.8-ms, voltage servo soft-start for each channel. When the ENx pin becomes higher than the enable threshold voltage, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start-up. When ENx becomes lower than the lower level of threshold voltage, TPS51225/B/C discharges outputs using internal MOSFETs through VO1 (CH1) and SW2 (CH2).

VREG5/VREG3 Linear Regulators

There are two sets of 100-mA standby linear regulators which output 5 V and 3.3 V, respectively. The VREG5 pin provides the current for the gate drivers. The VREG3 pin functions as the main power supply for the analog circuitry of the device. VREG3 is an *Always ON* LDO and TPS51225C has *Always ON* VREG5. (see Table 2 and Table 3)

Add ceramic capacitors with a value of 1 µF or larger (X5R grade or better) placed close to the VREG5 and VREG3 pins to stabilize LDOs.

The VREG5 pin switchover function is asserted when three conditions are present:

- CH1 internal PGOOD is high
- CH1 is not in OCL condition
- VO1 voltage is higher than VREG5-1V

In this switchover condition, three things occur:

- the internal 5-V, LDO regulator is shut off
- the VREG5 output is connected to VO1 by internal switchover MOSFET
- VREG3 input pass is changed from VIN to VO1

VCLK for Charge Pump

The 260-kHz VCLK signal can be used in the charge pump circuit. The VCLK signal becomes available when EN1. The VCLK driver is driven by VO1 voltage. In a design that does not require VCLK output, leave the VCLK pin open.

Overcurrent Protection

TPS51225/B/C has cycle-by-cycle over current limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS51225/B/C supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The CSx pin should be connected to GND through the CS voltage setting resistor, R_{CS}. The CSx pin sources CS current (I_{CS}) which is 10 µA typically at room temperature, and the CSx terminal voltage (V_{CS}= R_{CS} × I_{CS}) should be in the range of 0.2 V to 2 V over all operation temperatures.

The trip level is set to the OCL trip voltage (V_{TRIP}) as shown in Equation 3.

$$V_{TRIP} = \frac{R_{CS} \times I_{CS}}{8} + 1\,mV \tag{3}$$

The inductor current is monitored by the voltage between GND pin and SWx pin so that SWx pin should be connected to the drain terminal of the low-side MOSFET properly.The CS pin current has a 4500 ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the source terminal of the low-side MOSFET.

As the comparison is done during the OFF state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, can be calculated as shown in Equation 4.

$$I_{OCP} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{4}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it ends up with crossing the undervoltage protection threshold and shutdown both channels.

Output Overvoltage/Undervoltage Protection

TPS51225/B/C asserts the overvoltage protection (OVP) when VFBx voltage reaches OVP trip threshold level. When an OVP event is detected, the controller changes the output target voltage to 0 V. This usually turns off DRVH and forces DRVL to be on. When the inductor current begins to flow through the low-side MOSFET and reaches the negative OCL, DRVL is turned off and DRVH is turned on. After the on-time expires, DRVH is turned off and DRVL is turned on again. This action minimizes the output node undershoot due to LC resonance. When the VFBx reaches 0V, the driver output is latched as DRVH off, DRVL on. The undervoltage protection (UVP) latch is set when the VFBx voltage remains lower than UVP trip threshold voltage for 250 µs or longer. In this fault condition, the controller latches DRVH low and DRVL low and discharges the outputs. UVP detection function is enabled after 1.35 ms of SMPS operation to ensure startup.

Undervoltage Lockout (UVLO) Protection

TPS51225/B/C has undervoltage lock out protection at VIN, VREG5 and VREG3. When each voltage is lower than their UVLO threshold voltage, both SMPS are shut-off. They are non-latch protections.

Over-Temperature Protection

TPS51225/B/C features an internal temperature monitor. If the temperature exceeds the threshold value (typically 155°C), TPS51225/B/C is shut off including LDOs. This is non-latch protection.

External Components Selection

The external components selection is relatively simple for a design using D-CAP™ mode.

Step 1. Determine the Value of R1 and R2

The recommended R2 value is between 10 kΩ and 20 kΩ. Determine R1 using Equation 5.

$$R1 = \frac{\left(V_{OUT} - 0.5 \times V_{RIPPLE} - 2.0\right)}{2.0} \times R2 \tag{5}$$

Step 2. Choose the Inductor

The inductance value should be determined to give the ripple current of approximately 1/3 of maximum output current. Larger ripple current increases output ripple voltage, improves signal:noise ratio, and helps ensure stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{6}$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated as shown in Equation 7.

$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{7}$$

Step 3. Choose Output Capacitor(s)

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine ESR to meet required ripple voltage above. A quick approximation is as shown in Equation 8.

$$ESR = \frac{V_{OUT} \times 20\,mV \times (1 - D)}{2\,V \times I_{IND(ripple)}} = \frac{20\,mV \times L \times f_{SW}}{2\,V} \tag{8}$$

where

- D as the duty-cycle factor
- the required output ripple voltage slope is approximately 20 mV per t_{SW} (switching period) in terms of VFB terminal

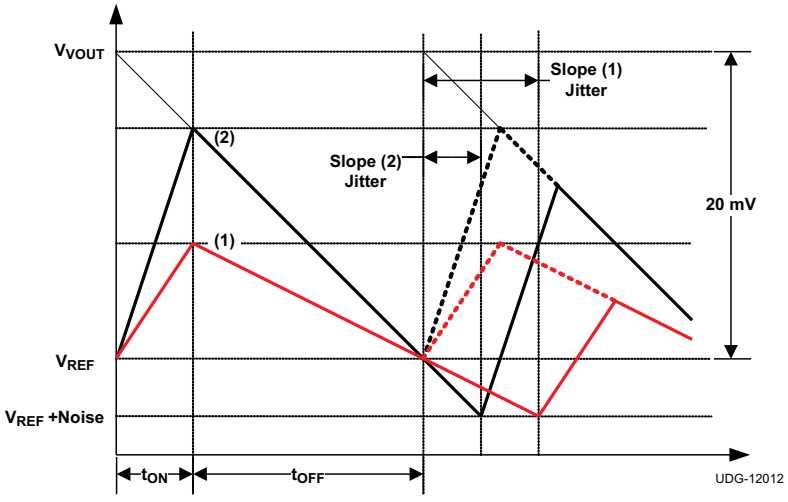


Figure 4. Ripple Voltage Slope and Jitter Performance

Layout Considerations

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout.

Placement

- Place voltage setting resistors close to the device pins.
- Place bypass capacitors for VREG5 and VREG3 close to the device pins.

Routing (Sensitive analog portion)

- Use small copper space for VFBx. There are short and narrow traces to avoid noise coupling.
- Connect VFB resistor trace to the positive node of the output capacitor. Routing inner layer away from power traces is recommended.
- Use short and wide trace from VFB resistor to vias to GND (internal GND plane).

Routing (Power portion)

- Use wider/shorter traces of DRVL for low-side gate drivers to reduce stray inductance.
- Use the parallel traces of SW and DRVH for high-side MOSFET gate drive in a same layer or on adjoin layers, and keep them away from DRVL.
- Use wider/ shorter traces between the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET
- Thermal pad is the GND terminal of this device. Five or more vias with 0.33-mm (13-mils) diameter connected from the thermal pad to the internal GND plane should be used to have strong GND connection and help heat dissipation.

TYPICAL CHARACTERISTICS

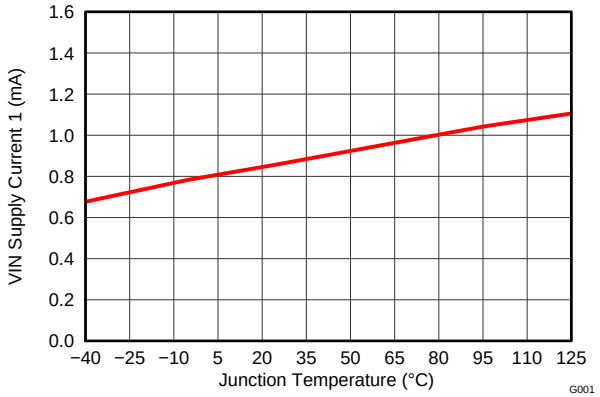


Figure 5. VIN Supply Current 1 vs. Junction Temperature

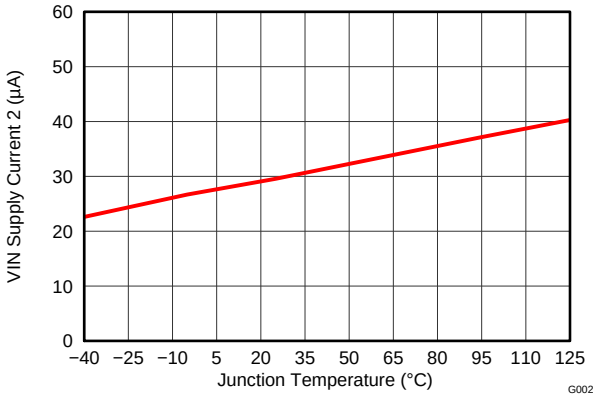


Figure 6. VIN Supply Current 2 vs. Junction Temperature

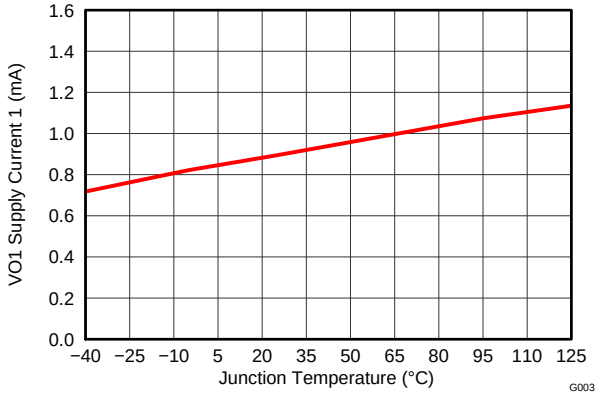


Figure 7. VO1 Supply Current 1 vs. Junction Temperature

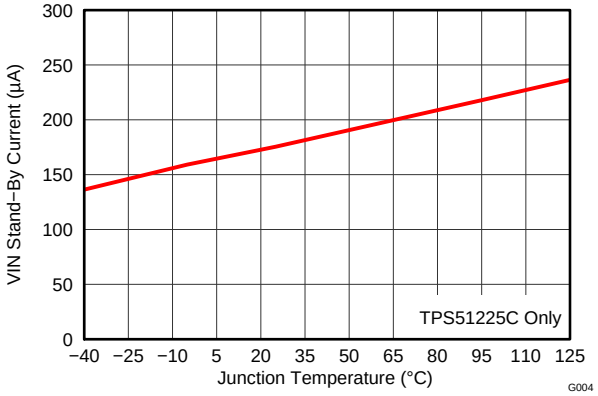


Figure 8. VIN Stand-By Current vs. Junction Temperature

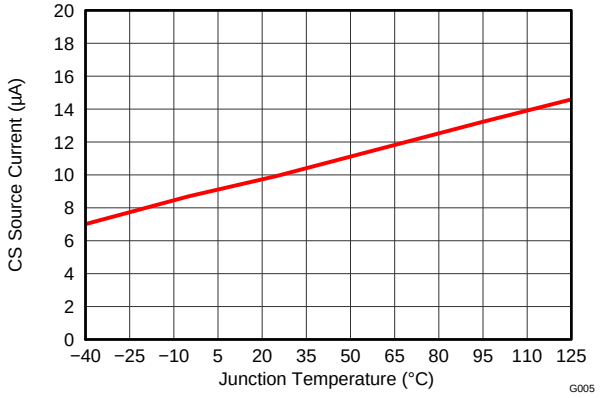


Figure 9. CS Source Current vs. Junction Temperature

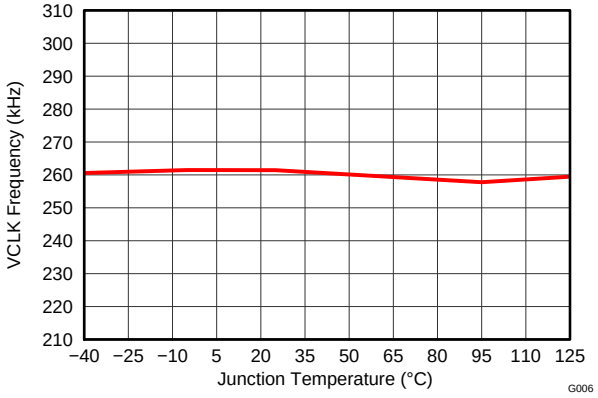


Figure 10. Clock Frequency vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

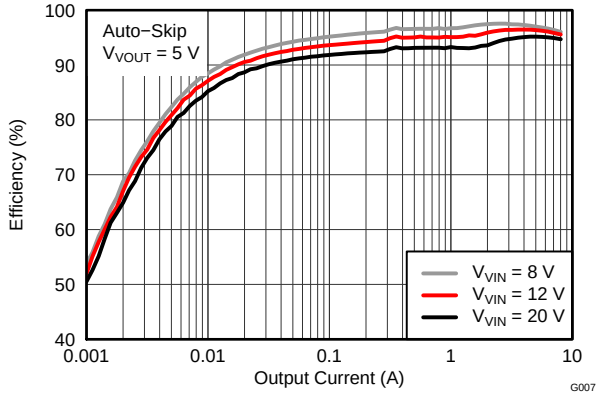


Figure 11. Efficiency vs. Output Current

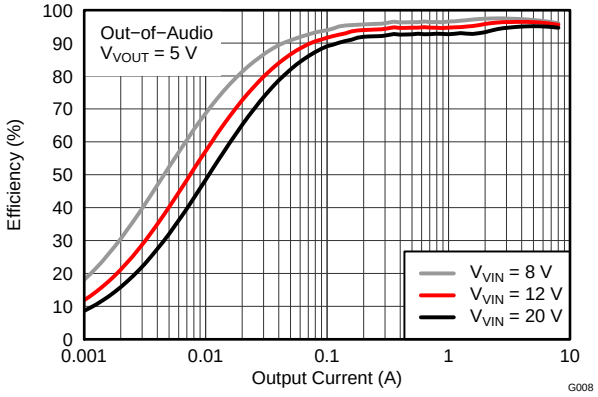


Figure 12. Efficiency vs. Output Current

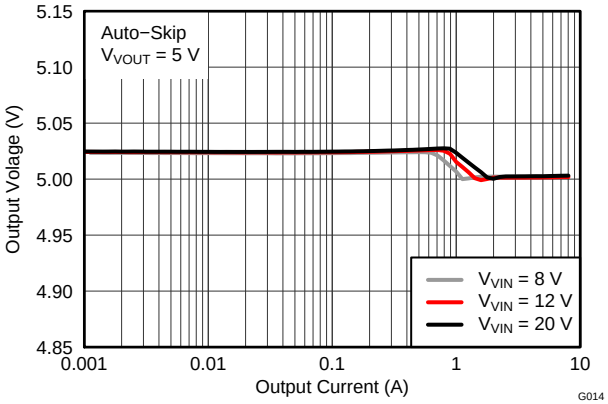


Figure 13. Load Regulation

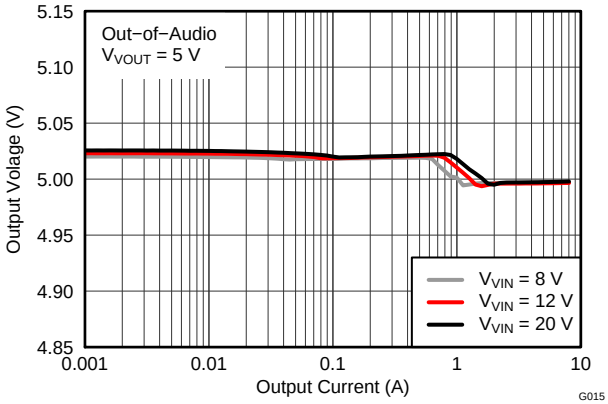


Figure 14. Load Regulation

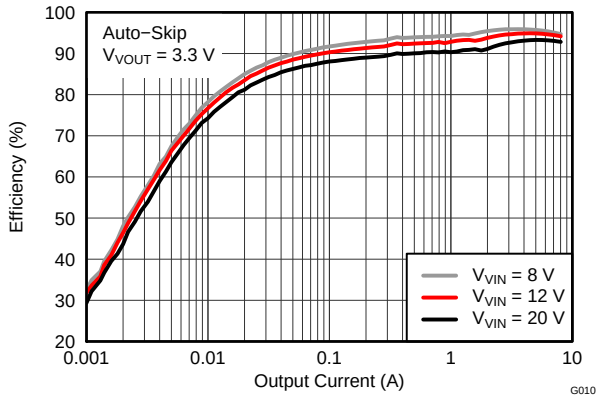


Figure 15. Efficiency vs. Output Current

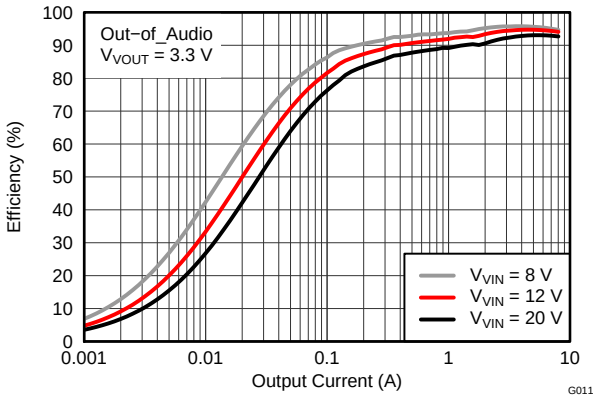


Figure 16. Efficiency vs. Output Current

TYPICAL CHARACTERISTICS (continued)

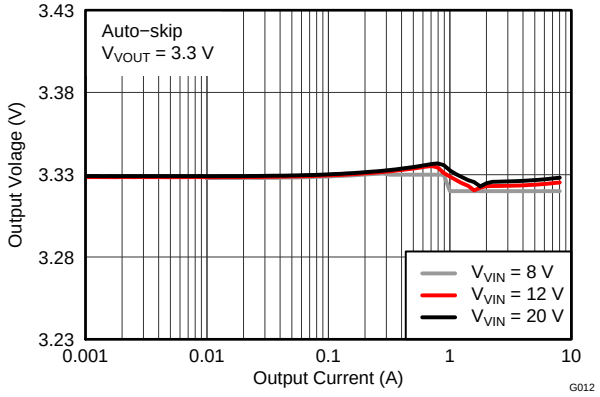


Figure 17. Load Regulation

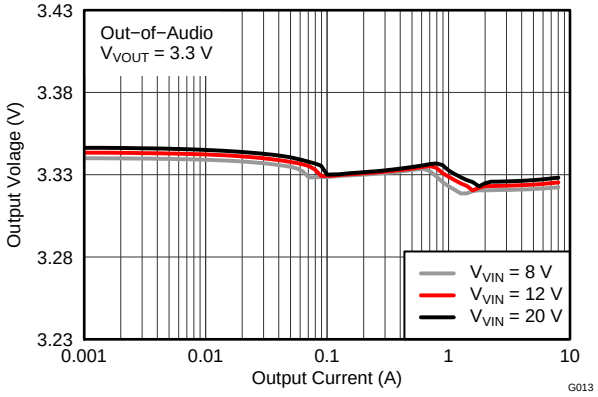


Figure 18. Load Regulation

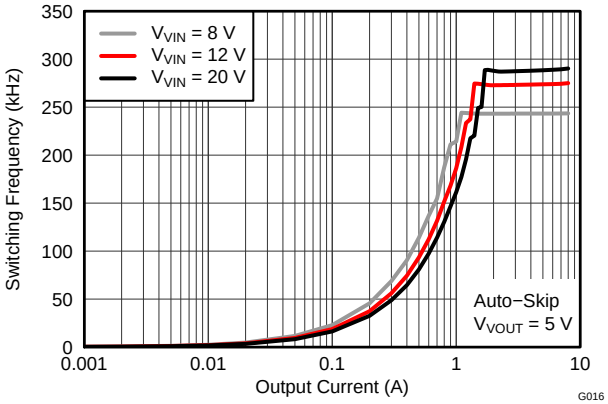


Figure 19. Switching Frequency vs. Output Current

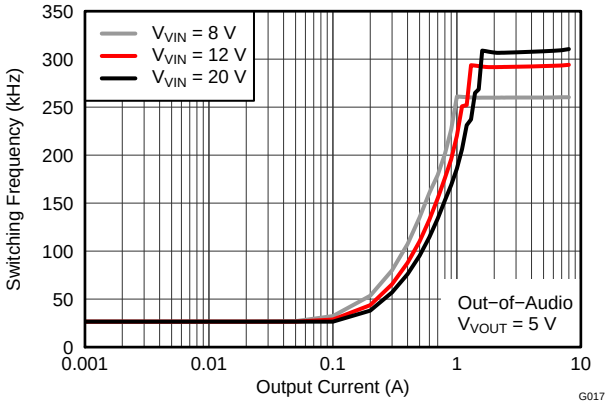


Figure 20. Switching Frequency vs. Output Current

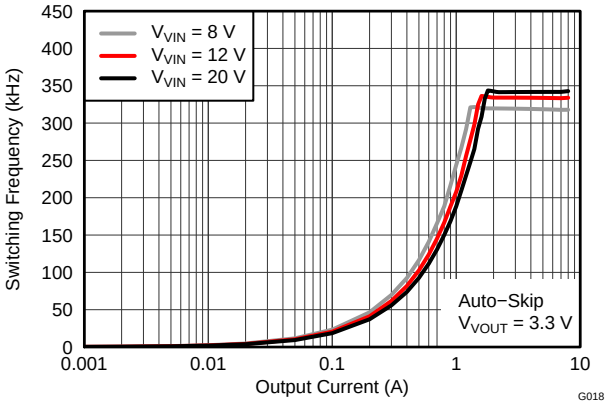


Figure 21. Switching Frequency vs. Output Current

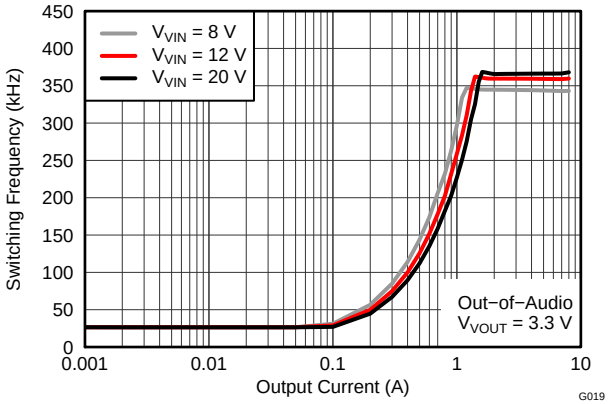


Figure 22. Switching Frequency vs. Output Current

TYPICAL CHARACTERISTICS (continued)

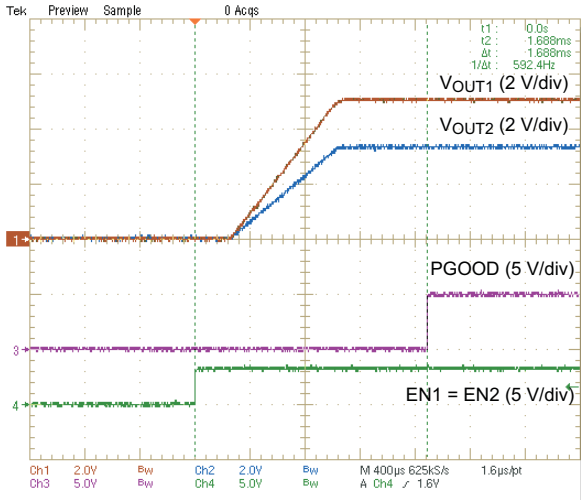


Figure 23. Start-Up

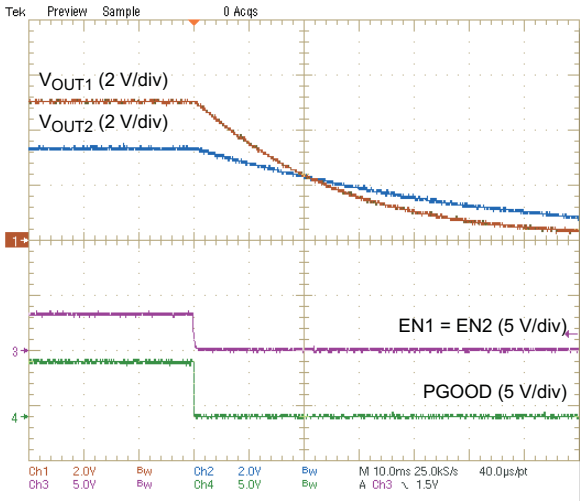


Figure 24. Output Discharge

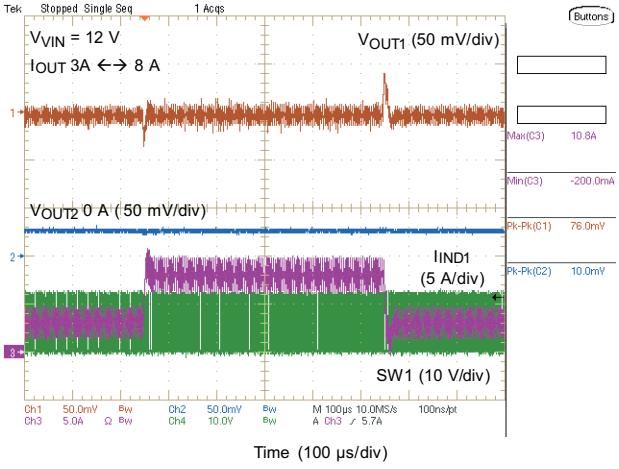


Figure 25. 5-V Load Transient

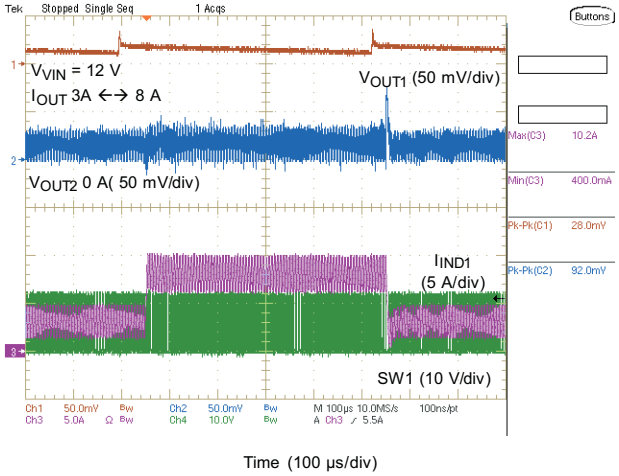


Figure 26. 3.3-V Load Transient

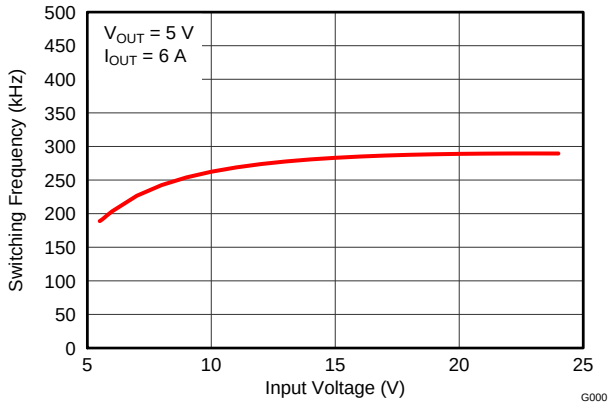


Figure 27. Switching Frequency vs. Input Voltage

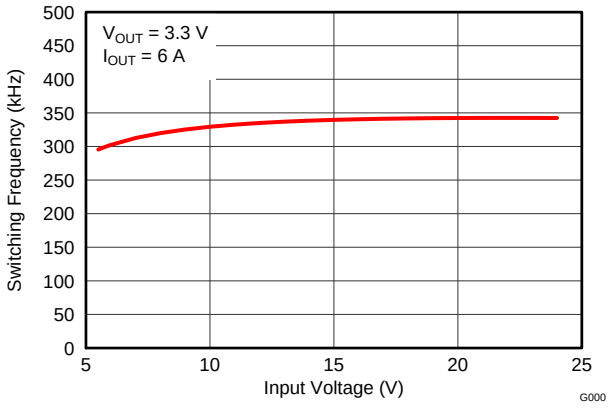


Figure 28. Switching Frequency vs. Input Voltage

APPLICATION DIAGRAM (TPS51225/TPS51225B/TPS51225C)

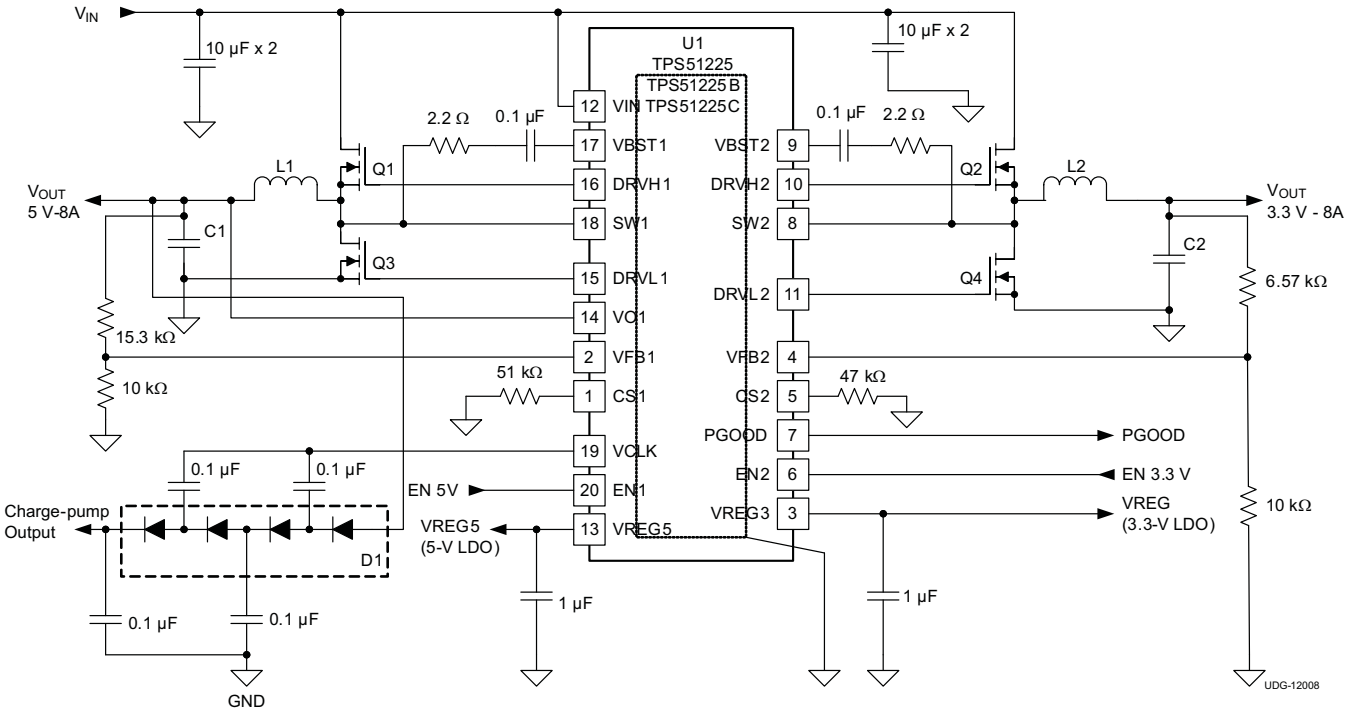


Table 4. Key External Components (APPLICATION DIAGRAM (TPS51225/TPS51225B/TPS51225C))

REFERENCE DESIGNATOR	FUNCTION	MANUFACTURER	PART NUMBER
L1	Output Inductor (5-V_{OUT})	Toko	FDVE1040-3R3M
L2	Output Inductor (3.3-V_{OUT})	Toko	FDVE1040-2R2M
C1	Output Capacitor (5-V_{OUT})	SANYO	6TPE330MIL x 2
C2	Output Capacitor (3.3-V_{OUT})	SANYO	4TPE470MIL
Q1	High-side MOSFET (5-V_{OUT})	Fairchild	FDMC7692
Q2	High-side MOSFET (3.3-V_{OUT})	Fairchild	FDMC7692
Q3	Low-side MOSFET (5-V_{OUT})	Fairchild	FDMC7672
Q4	Low-side MOSFET (3.3-V_{OUT})	Fairchild	FDMC7672

Changes from Original (January 2012) to Revision A **Page**

- Deleted references to obsolete option TPS51225A throughout document 1

Changes from Revision A (JUNE 2012) to Revision B **Page**

- Added specification for additional V_{VREG3} output voltage condition in ELECTIICAL CHARACTERISTICS table 5
- Added clarity to the VREG5/VREG3 Linear Regulators section. 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51225BRUKR	ACTIVE	WQFN	RUK	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1225B	Samples
TPS51225BRUKT	ACTIVE	WQFN	RUK	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1225B	Samples
TPS51225CRUKR	ACTIVE	WQFN	RUK	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1225C	Samples
TPS51225CRUKT	ACTIVE	WQFN	RUK	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1225C	Samples
TPS51225RUKR	ACTIVE	WQFN	RUK	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	51225	Samples
TPS51225RUKT	ACTIVE	WQFN	RUK	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	51225	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

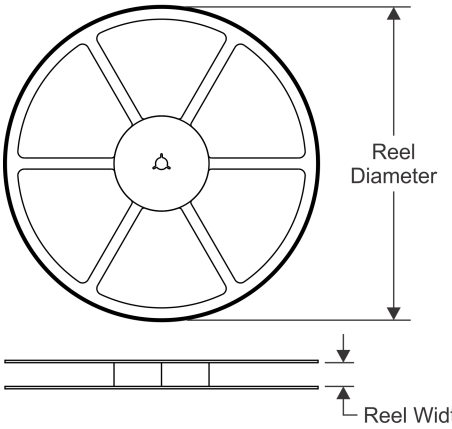
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

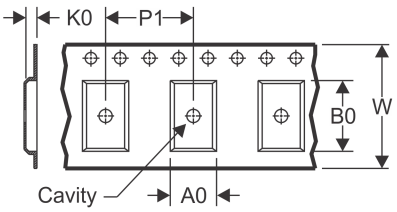
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

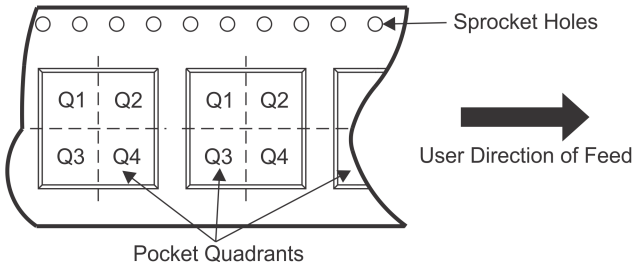


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

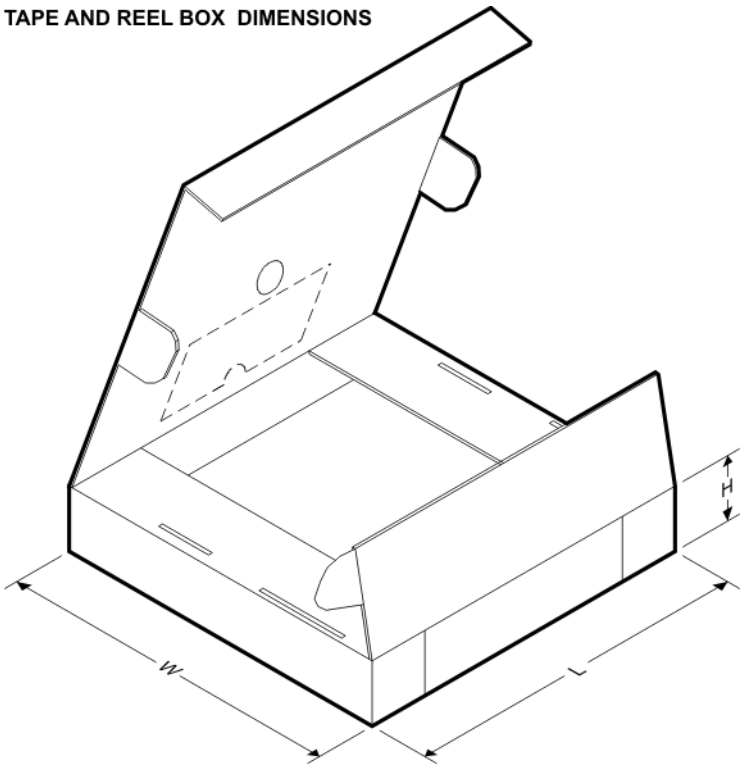
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51225BRUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51225BRUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51225CRUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51225CRUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51225RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51225RUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

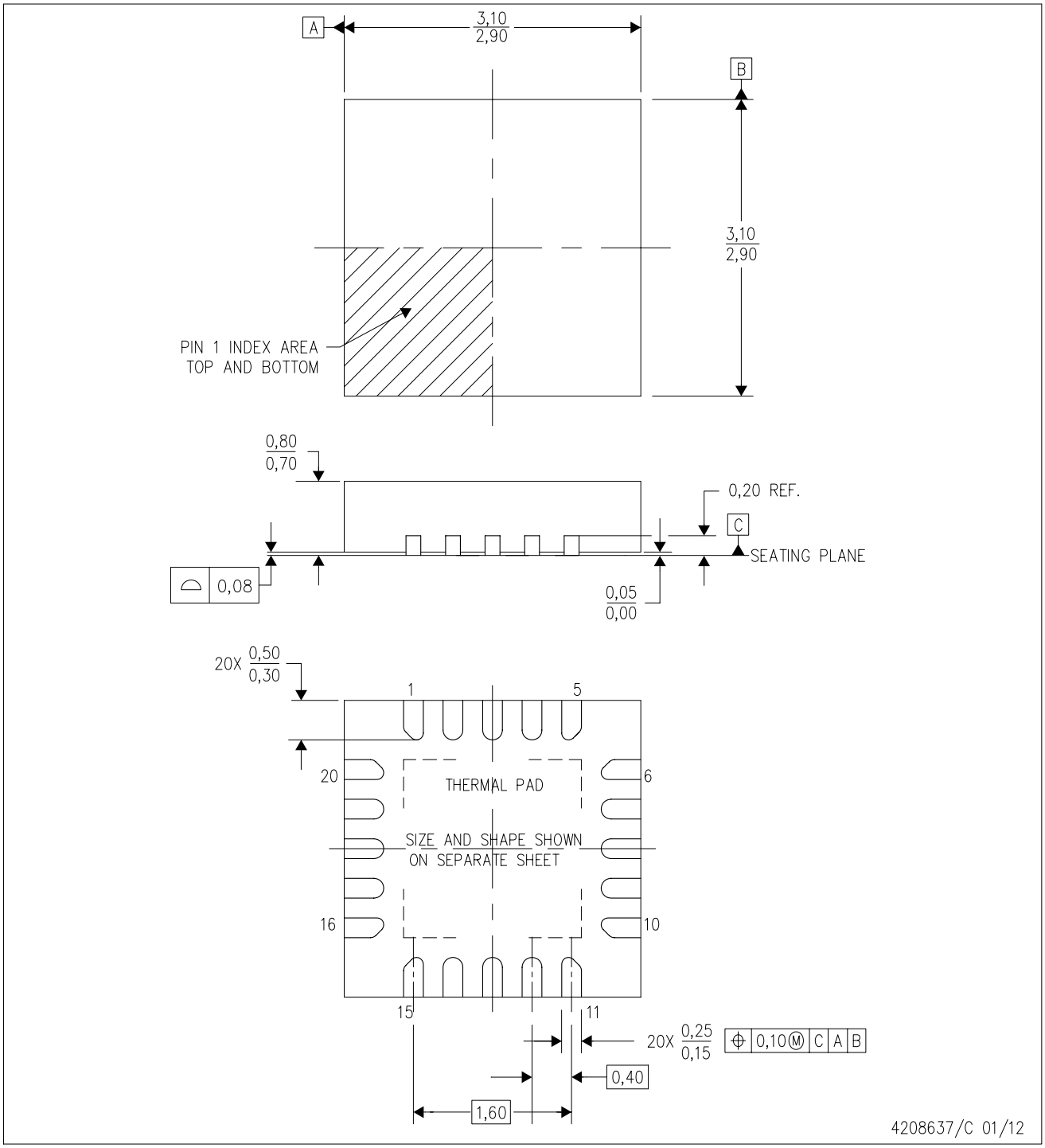
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51225BRUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
TPS51225BRUKT	WQFN	RUK	20	250	210.0	185.0	35.0
TPS51225CRUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
TPS51225CRUKT	WQFN	RUK	20	250	210.0	185.0	35.0
TPS51225RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
TPS51225RUKT	WQFN	RUK	20	250	210.0	185.0	35.0

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

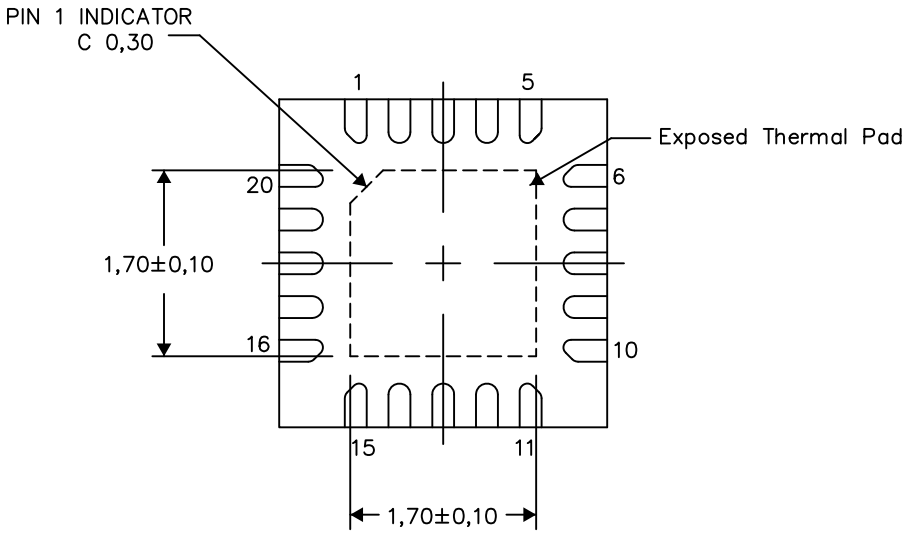
RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



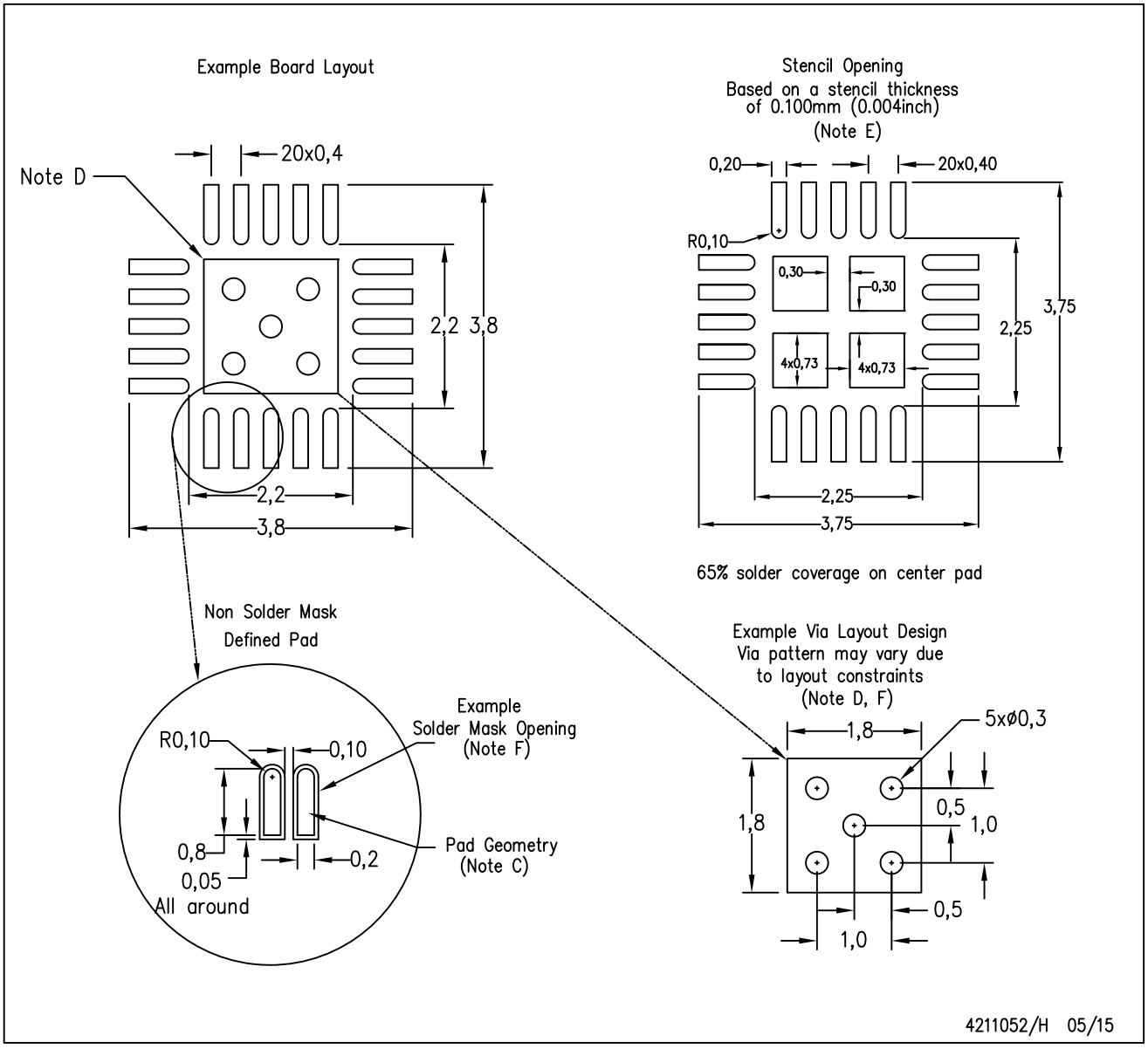
Bottom View

Exposed Thermal Pad Dimensions

4209762/I 05/15

NOTE: All linear dimensions are in millimeters

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265